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Analysis of temperature and high frequency effects in Double-Gate MOSFETs

Author:
Asmaa Masoud
اَسمَاء مَحمود مَسعود

Supervisor:
Prof: Benjamin Iñiguez

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بِسمِ اللهِ الرَّحمٰنِ الرَّحِيمِ

I would like to dedicate this thesis to:
Who first taught me how to live , to my Dad
the First person who introduced me to the wold of nanotechnology, to
Eng: Ahmed Abel Moteleb
To my supervisor and anyone who helped me in the progress of this thesis

THANK YOU ALL

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ABSTRACT

Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but nowadays with the ever increasing need for higher current drive and smaller sizes MOSFETS, hence cheaper. The scaling down had to come to an end because of its multiple problems like SCE (Short Channel Effect), so new technologies had to be introduced to solve this matter. SOI had shown better behaviour compared to bulk MOSFET as it helps reducing SCE by using a buried oxide. The most promising nowadays reducing SCE and increasing the scalability and giving better behaviour like more driving currents and better sub-threshold slopes are MUG FETS (MUltiple Gating FETS) which introduce better control of gates over channel hence reduce DIBL, leakage current and improve the overall performance.

In this thesis we are focusing more on DG MOSFETS(Double Gate) as The DG-MOSFET seems to be a good candidate to meet the International Technology Road- map (ITRS-2009) requirements for high-performance logic technology. so we made simulation analysis of DG mosfets performing in both high temperature and high frequency to prec=dict how they behave under those circumstances due to further applications for them in extended Thz applications.

This thesis is organized as follows, in Chapter(1) we are giving an introduction about the history of downscaling and the SCE and how to continue following the roadmap with introducing new ideas and technologies, while in Chapter(2) we are focusing on our interest of search (DG MOSFETS) and how they behave with high frequency and high temperature and how they introduce a good candidate to the future of low power, high frequency applications. Finally in Chapter(3) we include our simulation results showing how the behaviour of a DG MOSFET model is affected by high temperature and high frequency at the same time. The results are pretty interesting as there are new and no one before has searched this point.

CHAPTER ONE

1. INTRODUCTION

1.1 Roadmap

since the introduction of integrated circuits(ICs)in 1958, engineers and researchers around the world are working on how to add more speed, better performance and smaller chips. The semiconductor industry has made considerable progress, add to account the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). the main goal is to follow the road map called Moore's law. Moore's law is named after Intel co-founder Gordon E. Moore. In 1965 he described the trend in his paper. The paper noted that the number of components in integrated circuits had doubled every year from the invention of the integrated circuit in 1958 until 1965 and predicted that the trend would continue "for at least ten years", then in 1975 it was updated to "the number of of components double every two years". Fig 1.1

The ITRS (International Technology Roadmap for Semiconductor) had been tracking the progress of the semiconductors as illustrated in Fig 1.2 in order to identify critical challenges, encourage innovative solutions, and welcome participation from the semiconductor community.

1.2 Downscaling

In order to follow the aforementioned roadmap, new solution had been introduced. Downscaling was the main method for resulting better device density and performance. For a long period shrinking the size with the same planar bulk mosfet was adopted due to the low cost and excellent scalability. Accroding to the ITRS roadmap at some point the scaling faced some serious problems which leaded to the appearance of new technologies in parallel with downscaling as the downscaling approached physical limitations according to the noise behaviour of extra small devices, namely those technologies are SOI MOFET (Silicon On Insulator) dates back to 1964 with PD (partially Depleted) and FD (Fully Depleted) behaviour related to the manufacture procedure [1], Multiple gating (as in order to gain back the control of the

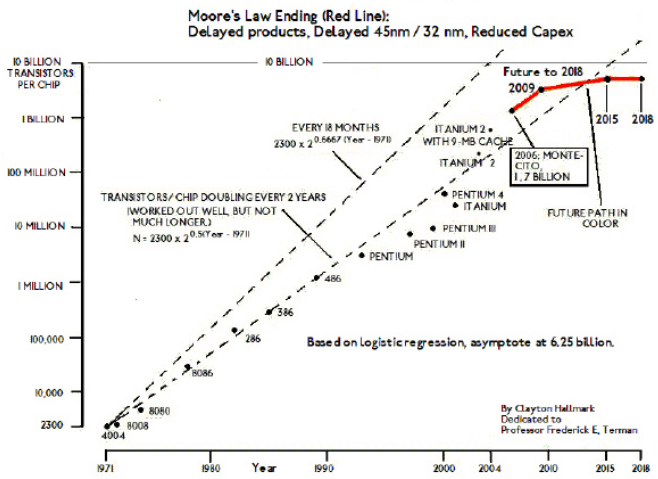


Fig. 1.1: Moore's law

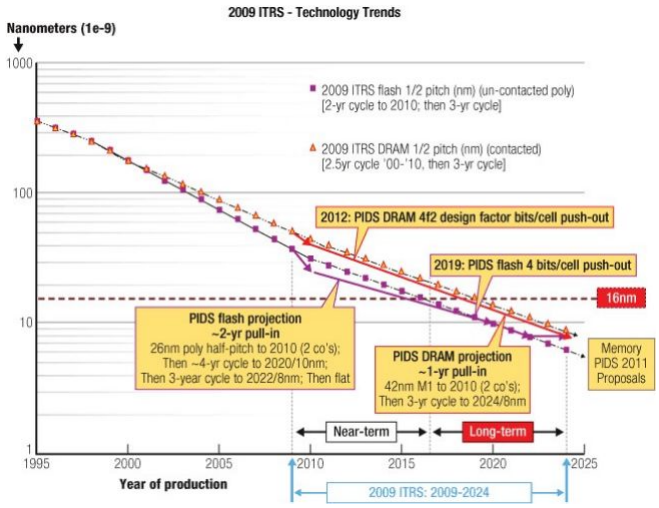


Fig. 1.2: ITRS roadmap 2009

channel and reduce the DIBL noise)and SiGe Technology which suggest the usage of new materials while implementing the main Mosfet Materials [2].

1.2.1 Multiple gates

In an increasing need to obtain higher driving current and better short channel characteristics SOI technologies had to shift from normal, planar and single gate fabrication to three dimension fabrication with multiple gates (double-, triple- or quadruple-gate, GAA and π gate devices)Fig1.3 [3] in Fig1.4 show the family tree. The first fabricated double-gate SOI MOSFET was the fully DEpleted Lean-channel TrAnsistor (DELTA, 1989). From this first device it was shown by simulation that it has better behaviour over Bulk planar ones represented in better sub-threshold slope, current drive and transconductance.

The word "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor. so what are those multiple-gates offering over the single gate?
The key-word here should be short channel effects (SCE)
SCE is the main problematic issue for downscaling and it has several impacts on the total behaviour of the devices. Such problems are Drain Induced Barrier Lowering (DIBL), surface scattering, velocity saturation, impact ionization and hot electrons. the muli-gating techniques apply more control of the gate over the channel and reduce the leakage current caused by the shrinkage in size and therefore improve the sub-threshold curve and the on-off switching.

1.2.2 Short channel effects

A mosfet can be considered as a short channel when the channel length comes to the same order as the depletion layers width (x_{dS}, x_{dD}), which are the source and drain depletion layers. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise.
There are five considerable short channel effect should be taken into account while studying any MOS behaviour [4]and those are:

1. Drain-induced barrier lowering and punch-through
2. Surface scattering
3. Velocity saturation

4. Impact ionization

5. Hot electrons

Drain-induced barrier lowering and punch-through: this problem happens when the channel is too short then not only the Gate voltage (V_{GS}) which it controlling the barrier voltage of the channel but also the Drain voltage(V_{DS}) then the depletion layers mentioned before (x_{dS}, x_{dD}) get closer to

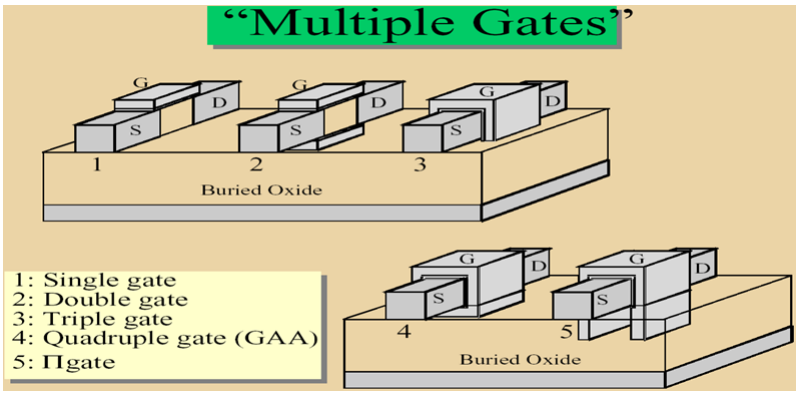


Fig. 1.3: Mutliple gate devices

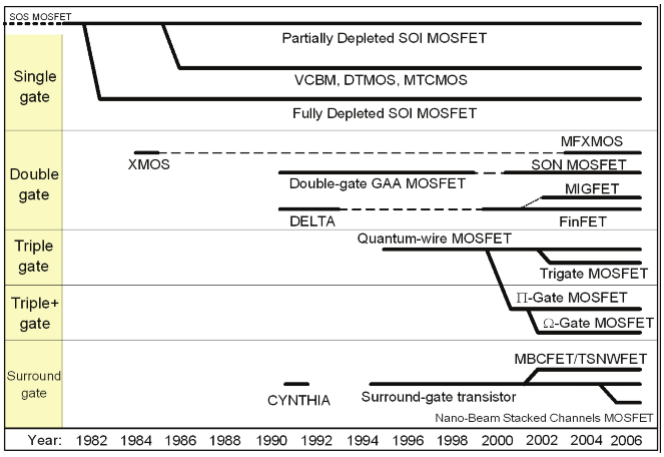


Fig. 1.4: SOI mosfet family tree

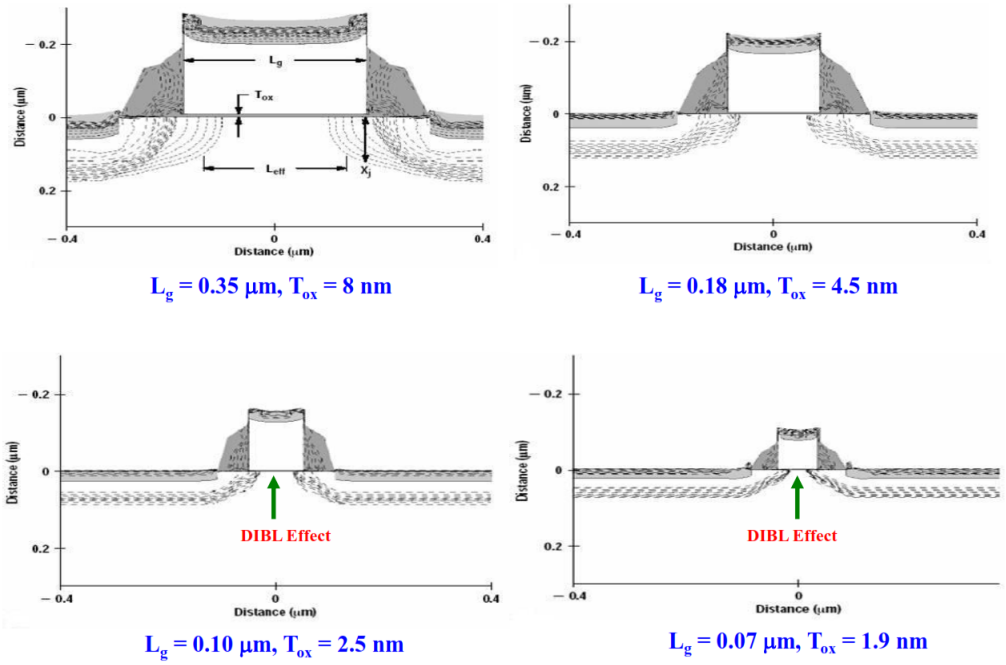


Fig. 1.5: The effect of DIBL

each other that the Gate completely lose the control over the channel (according on how much the channel is small). those depletion layers can be mathematically expressed as:

$$X_{dD} = \sqrt{(2\epsilon_{si}\frac{q}{N_A})(V_{DS} + \phi_{si} + V_{SB})} \tag{1.1}$$

$$X_{dS} = \sqrt{(2\epsilon_{si}\frac{q}{N_A})(V_{DB} + \phi_{si})} \tag{1.2}$$

Therefore when any voltage is applied on the Drain, Source ends it causes a leakage current to travel through the channel despite there is a voltage applied on the Gate end or not Fig**??**1.5. This flow of current while Gate loses control make a new condition called sub-threshold current, which is the current that flows even though $(V_{GS}) < (V_{T0})$, (V_{T0}) is the threshold voltage.

Surface scattering: it is mainly caused by the lateral field forcing new domination on the channel. This field cause the electrons to be accelerated in the Y direction while it is originally controlled by the vertical field ε_x Fig1.6 which leads to the more collisions between the electrons that reduces their mobility.

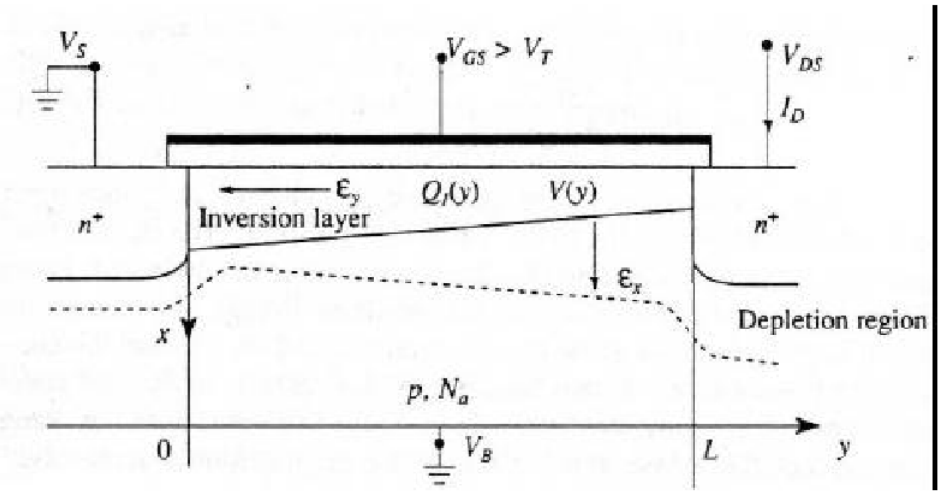
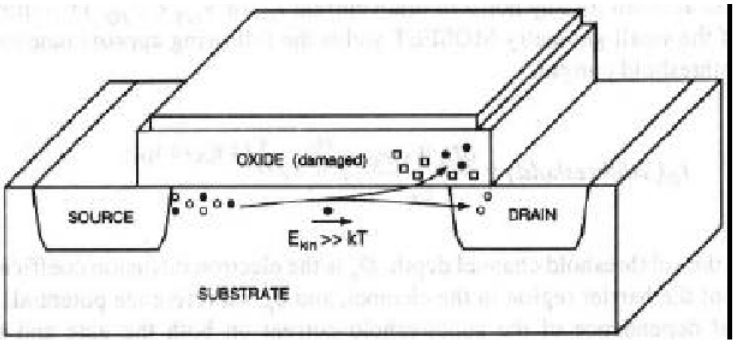


Fig. 1.6: Fields affecting electrons mobility



carriers.png

Fig. 1.7: Hot carriers in oxide

Velocity saturation: Velocity saturation occurs when the voltage applied on the Drain-Source end increase beyond the limits of the saturation voltage,at this point the drift velocity also saturates but in according to short channel effect this procedure happens faster.

Impact ionization: another undesirable short channel effect, which almost happens in N-channel mosfets. in this Phenomenon occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole $(e-h)$ pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them.

Hot electrons: the so-called Hot electrons Phenomenon is caused by high electric field which cause high-energy electrons that might enter the oxide and kept trapped there Fig1.7. this is a problem as with time those electrons can accumulate in the oxide and charging it, as the oxide gain some charge this increase the threshold voltage V_T and affect adversely the gate's control on the drain current.

1.3 Advantages of SOI, DG and MG

The advantages of each of the aforementioned technologies relay on how they help reducing or eliminating short channel effects, so for SOI(Silicon on insulator) the way SOI solved SCE is by using buried oxide to reduce the electric field caused by Drain-Source ends, as instead of propagating the electric field lines through the channel it propagates through the oxide Fig1.8 hence reduce the control of that field over the channel. SOI is especially suited for low power applications, the technology has spread to the analog world, being a serious option for low-cost analog/RF products, such as front-end receivers of mobile phones. Though that buried oxide helped to reduce the effect of short channel, scientists and researchers found that this technique is not enough to follow up with the roadmap. New technologies kept to appear to offer more options for shrinking the size and still progressing higher performance. Double gates and Multiple gates have higher control of gates over the channel by applying in fabrication stage over steps which is adding more gates. This new structure offer theoretically the best control of the channel region. In consequence of the better control of the channel some advantages had appeared such(increased mobility hence increased current drain current, Volume inversion phenomenon and Speed superior).

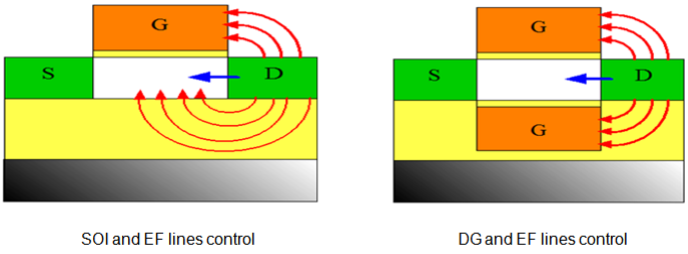


Fig. 1.8: SOI and DG controling EF from Drain technique

CHAPTER TWO

2. DG MOSFET WITH TEMPERATURE AND HIGH FREQUENCY

In this chapter a preview about Double Gate mosfet structure and behaviour based on temperature and high frequency will be introduced. The most important is to show how high temperature high frequency can affect the main MOS behaviour according to

2.1 Structure

In normal operation of any MOS device, the goal is to control the flow of charge carriers through the channel. this control comes basically from the Gate end which happens as next; while applying voltage on Gate end this lowers the voltage barrier of the channel between Drain and Source ends. Hence a channel is created allowing the carriers to flow in it after applying voltage on the other two ends. when there is no voltage applied at the gate the current flow should be zero.

Now it is rather clear the importance of gate end, but while shrinking the size of MOS devices this control was lowered by the external field caused by drain and source depletion layers and to retain this control over the channel the new Multiple gate techniques had appeared to do so. Talking about Multiple-gate devices or so-called (MUG-FETs) there is one promising device among them specially in the analog low power application. This device is DG MOS (Double-Gate MOSFET).

the basic structure of DG mosfet, as IBM's Wong illustrates " there are three ways to build a Double Gate mosfet" [5] "You can do it horizontally (a) with one gate on top and another on the bottom. You can do it vertically(b) so that the current runs perpendicular to the silicon surface, or you can do it with the channel and gate perpendicular to the surface (c) but with the current parallel to the surface" Fig2.1.

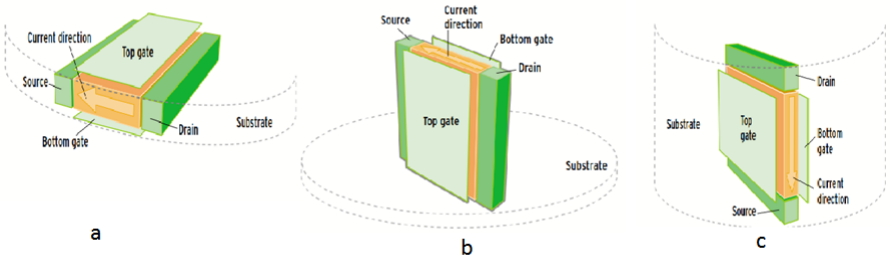


Fig. 2.1: Double gate different structures

2.2 Double gate modelling

There had been a lot of work done modelling DG mosfet. The importance of modelling new devices is to get the closest circuit that precisely simulate their behaviour in order to add them to different simulating tools.

Nano-scale Double Gate mosfet has a lot of challenges to face encountered in enhanced coupling between the electrodes source drain and gates, quantum confinement, ballistic or quasi-ballistic transport, gate tunnelling current, etc. Most of models introduced are for undoped or lightly doped devices with long enough channel to assume that the transport of current is due to drift diffusion, regarding this most of models were made in (1D) Poisson equation neglecting the effect of the lateral field imposed with shrinking the size and cause SCE. In particular Double Gate was mainly developed to maintain the SCE, Taur et lu [6]have derived expressions for the I-V characteristics for these devices using formula that required the solution of a transcendental equation for an intermediate function β. this transcendental equation needs to be solved numerically, but such solutions makes it harder to be used in tools like SPICE. Morris and Cumberbatch [7] became to new solution using (LAMBERT W Function) together with the first evaluation of TAUR and LU. Their results had shown to be accurate compared with exact numerical solutions.

Still all those solutions for undoped or slightly doped DG devices, it is absolutely necessary to add all the effect of short channel in order to lead to further studies on Frequency or temperature behaviour which is also affected with SCE.

Adding short channel effects to the analytical solutions shows the necessity of solving 2D dimension Poisson equation as well instead of Drift-Diffusion (DD) modelling Hydro-Dynamic (HD) modelling should be used

according to the advantages it gives over (DD) modelling mentioned in [8].

In [9], this paper presented a compact model for rf/noise applications including quantum effects and hydrodynamic transport. A comparison between drift-diffusion model and non-stationary model was presented as well.

2.3 Temperature effects on DG MOSFET

The effect of Temperature has become more countable specially after scaling down and gathering huge number of transistors into single chip. Those transistors working together added to high frequency leads to high temperature induced, so it became too important to investigate the effect of this temperature on devices behaviour.

Temperature has effect on different areas in MOS, most important is Threshold voltage (V_t) and Mobility (μ) and velocity saturation (V_{sat}), each of those will be illustrated individually.

2.3.1 Temperature effect on threshold voltage

First, the effect on (V_t), this effect comes from the temperature dependence of the surface inversion potential induce changes in threshold voltage over temperature. Between -100 C to 100C, the threshold voltage temperature coefficient is

$$TCV_{THN} = \frac{1}{V_{THN}}.\frac{dV_{THN}}{dT} \approx -3000PPM/C \tag{2.1}$$

and then threshold function is affected by this change by

$$V_{THN}(T) = V_{THN}(T0)[1 + TCV_{THN}.(T - T0)] \tag{2.2}$$

on the other hand it is evident that the 2D charge density ni in each subband is increases proportionally with temperature. This in turn increases the sub-band current for that longitudinal energy. As a result, the total ballistic drain current is increased and the threshold voltage (V_t) is simultaneously reduced. This study was made on high-κ gate stack Double Gate MOSFET in [10], also it has been verified that the sub-threshold slope increases proportionally with operating temperature.

2.3.2 Temperature effect on Mobility

The temperature effect on mobility appears directly from μ basic equation:

$$\mu_T = \mu_{300K}.[\frac{300K}{T}]^{\alpha} \tag{2.3}$$

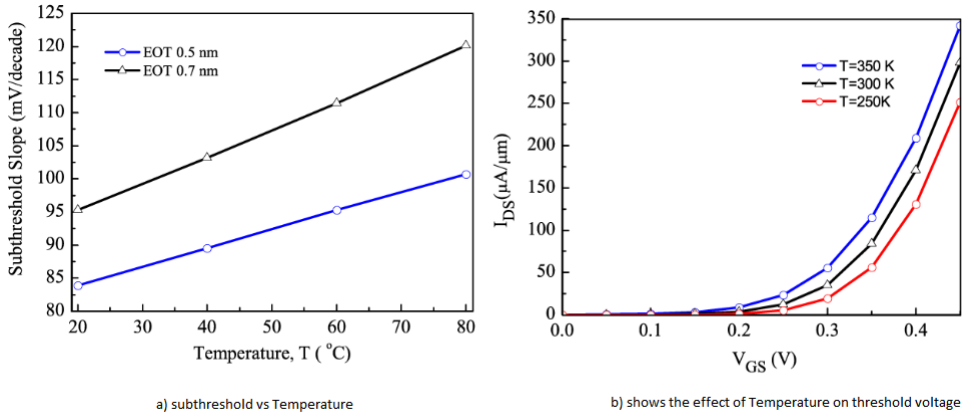


Fig. 2.2: Temperature effect on a)sub-threshold slope b) threshold voltage

where α is a coefficient $1 < \alpha < 0$ which declare that the Mobility is highly affected by temperature and with the increase of temperature over temperature room the mobility will be degrading. However at low-drain currents the variations in surface inversion potential (affecting the threshold voltage) with temperature will dominate the temperature-induced changes in drain current. At higher drain currents the mobility temperature dependence will dominate. The reduction of Mobility affect MOSFET in different aspects, one important aspect is g_m the MOS transconductance is the gain and it can be expressed as

$$g_m = [\frac{\Delta I_{DS}}{\Delta V_{GS}}]_{V_{DS}} \tag{2.4}$$

and related to temperature it can be expressed as

$$g_m(T) = g_m(300K)[\frac{T}{300}]^{-\frac{2}{3}} \tag{2.5}$$

and this reduction is due to the reduction of mobility as the temperature increases.

As well the velocity saturation V_{sat} is affected by mobility degradation with temperature as the velocity of electrons equation is:

$V_n = \mu_n E(X)$, it is supposed that the stronger the electric field across the channel, the higher the velocity (and faster the device), but with the effect of mobility the velocity reaches the V_{sat} earlier.

there are some effects of parasitic on devices are usually described as thermal noise and they can be inserted to the circuit as current sources.

2.4 Frequency behaviour of DG Mosfet

The unique structure of DG mosfet has caused them to be able to exhibit excellent analog/RF behaviours. the important figure of merit of MOSFETs for analog integrated circuits are drain current, I_{ds}, transconductance, g_m, output conductance, g_{ds},(intrinsic/open loop gain), g_m/g_{ds}, the g_m/I_{ds} ratio,etc. Comparing DG devices behaviour with UTB (Ultra Thin Body) SOI as mentioned in [11] in this paper a study was made to compare between them in order to show how DG outperform on other new technologies such UTB SOI.

The simulation results showed that DG device can provide larger drive current and higher carrier mobility than UTB SOI, as well for transconductance, etc.

A closer look to the high frequency behaviour of any mosfet we find that there are two most important figure of merits F_t and F_{MAX} are the transition frequency and maximum oscillation frequency respectively. Transition frequency is the frequency when the current gain is in unity. It is an interesting criterion for high-speed digital applications where speed and high swing are concerned, it can be represented as follows:

$$F_T = \frac{g_m}{2n(c_{gs} + c_{gd})} \approx \frac{g_m}{2nc_{gg}} \tag{2.6}$$

where g_m is the transconductance and c_{gg} is the gate capacitance of the device. According to the equation it is quite obvious to maintain higher values of F_T depends on achieving higher values of g_m and lower of c_{gg} those two could be enhanced by structure, hence DG gives higherg_m .

The maximum oscillation frequency is a figure of merit related to the capability of the device to provide power gain at large frequencies, and it is defined as the frequency at which the magnitude of the maximum available power gain drops to unity.

$$F_{MAX} = \frac{F_T}{2\sqrt{(R_g + R_s + R_i)(g_{ds} + g_m\frac{c_{gd}}{c_{gs}})}} \tag{2.7}$$

This equation shows the strong relating between F_{MAX} and g_m but in this case is lowering relation. As if g_m grows higher F_{MAX} drops lower, even though still DG mosfets shows higher F_{MAX} compared to other devices as for this lowering is not compared to the height of F_T and low g_{ds}.

By simple analysis based on lumped elements Noise figure can be calcu-

lated for DG mosfet from the equation:

$$NF_{min} = \frac{F}{F_T}\sqrt{g_m(R_g + R_s)} \tag{2.8}$$

Equation shows that the minimum noise figure is strongly dependent to transconductance and transition frequency. a smaller NF_{min} can be obtained in the DG MOSFET. Although large values of gm in DG devices would cause to the increasing inNF_{min} , but it had been compensated by larger transition frequency that scale up in a faster rate than the effect of transconductance, which shows the potential of the structure for low-noise operations.

following Fig2.3 show the behaviour of DG mosfet compared to UTB SOI devices obtained from [11].

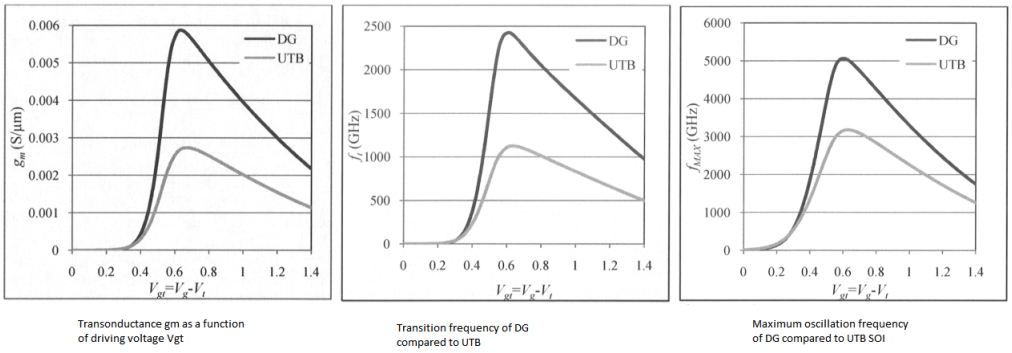


Fig. 2.3: Comparison between DG and UTB SOI RF behaviour

2.5 Temperature Dependent RF Performances

In this section, a spotlight will be made on aforementioned relationships about temperature and frequency. It was obvious mentioning temperature effect on DG devices that the major concern was about mobility μ and threshold voltage V_t, meanwhile in frequency dependence figure of merits were transconductance g_m, transition frequency F_T, maximum oscillation frequency $F_{MAX}$and minimum noise figure NF_{min} . In order to study how temperature affect RF behaviour of DG mosfets or any kind on mosfets it is momentous to show how those factors are related and what yields from this relationship on the behaviour of DG mosfet in RF frequency regions.

In 1999 [12], it was shown throw the aforementioned relations of those figure of merits that there is a proportional relationship from measurements and simulation of RF-CMOS devices shown as ($F_T \propto T^{-K}$) which shows the relation between transition frequency and operating temperature, as well ($F_{MAX} \propto T^{\frac{-K}{2}}$) that shows the relation between maximum frequency and temperature. Since F_T and F_{MAX} are proportional to g_m and $\sqrt{g_m}$ respectively, so the empirical temperature dependence can have the same relation.

CHAPTER THREE

3. RESULTS AND CONCLUSION

When devices are miniaturized into the nano-meter scale regime nowadays, some challenges abound. Some challenges are new, some are just getting tougher and most of them will continue to become even more difficult to deal with for future. The main goal of this thesis is to study some of those challenges for DG devices, for what those devices show as promising devices for the future of downscaling of CMOS technology specially due to the unique structure of double gate (DG) devices, it can exhibit excellent analog/RF behaviors. Higher g_m/Ids ratio and intrinsic gain, g_m/g_{ds} can be received by them. Superior F_T and F_{MAX}, which are due to higher transconductance, g_m and lower output conductance, g_{ds} , can be observed in the double gate devices. In addition, better noise and gains performance can be achieved resulting from improved g_m . Thus, Double gate devices can be considered as better candidates for analog/RF applications.

A compact model of double-gate-metal-oxide-semiconductor field-effect transistor was used in this thesis in order to investigate the RF/temperature behaviour of this kind of devices. this model can be found in [9] where an analytical model for high frequency and microwave noise model of nano-scale double-gate metal-oxide-semiconductor field-effect transistor was presented. The model is based on a compact model for charge quantization within the channel and it includes overshoot velocity effects. Radio-frequency and noise performances are calculated using an active transmission line method.A comparison is made between classical and quantum charge control and between drift diffusion and hydrodynamic models.

3.1 Experimental results

3.1.1 Testing conditions

The testing conditions for this simulation was to set a big range of temperature and frequency, in order to predict all possibilities of DG mos behaviour either in high temperature low frequency or low temperature low frequency, etc. The most important result that attain our concern is high frequency high temperature effects, so we made a range of temperature between room temperature 27$c$and 150c and for frequency from 10GHz to 100GHz, Gate

voltage relays in between $0.5 < V_{gs} < 2$ Volts and we setV_{ds} to zero.

3.1.2 Measurements and calculations

The code we have simulating DG MOSFET is already calculating Y and S parameters. The method of calculation is mentioned in [13]. From this code we obtain $Y_{11}, Y_{12}, Y_{21}, Y_{22}$. The input and output impedances can be obtained easily from those figure of merits, as we are considering the channel as a transmission line and from [14]. so we get

$$Y_{in} = \frac{i_1}{v_1} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \tag{3.1}$$

and

$$Y_{out} = y_{22} - \frac{y_{12}y_{21}}{y_{11} + Y_S} \tag{3.2}$$

from those two equations 3.1 and 3.2 we can calculate input and output impedances as:

$$Z_{in} = Y_{in}^{-1} \tag{3.3}$$

$$Z_{out} = Y_{out}^{-1} \tag{3.4}$$

then from equation 3.4 we calculated R_{out} as the real part of Z_{out}.

3.1.3 Simulation results

In order to check for RF/temperature behaviour of this model it was important to verify whether the temperature dependences in the code are correctly introduced. The vital parameters that change with temperature are :

1. Threshold voltage(V_{th}): From relations of threshold voltage and temperature, it was expected that the threshold voltage will degrade with the increase of the temperature linearly which was proved with the following graph:
   Fig. 3.1.In this graph, we can see that the relation ship is almost linear which satisfy the promising results and assure that the code used is describing the voltage-temperature relation correctly.

2. Mobility(μ): As aforementioned in section 2.3.2, the relation between mobility and temperature. the expected result of this relation that the mobility is degraded with the temperature grows high which was the exact result of the code shown in Fig. 3.2

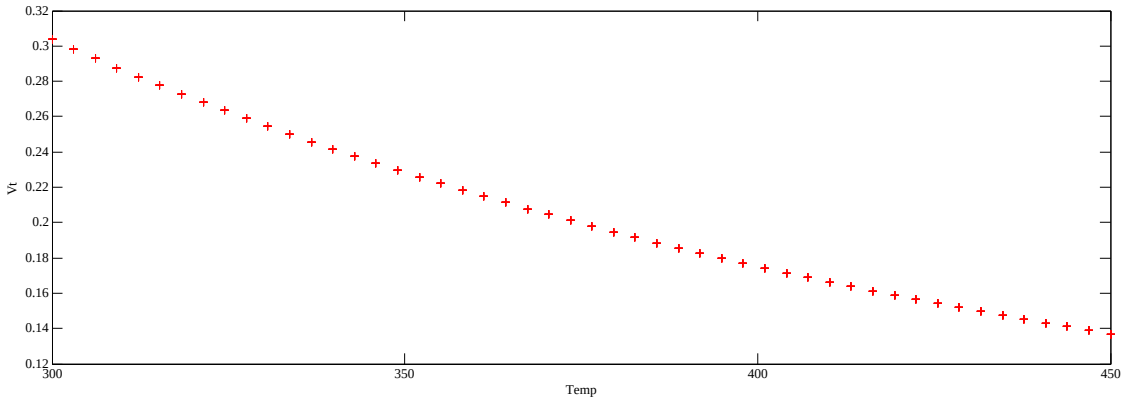


Fig. 3.1: Threshold voltage Vs Temperature with $V_{ds} = 0$

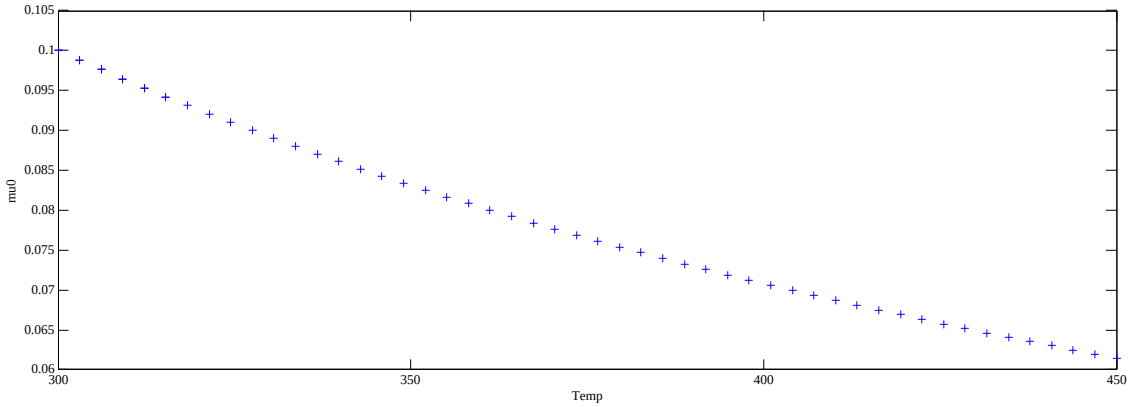


Fig. 3.2: Mobility Vs temperature

Output impedance

Output impedance one of the main characteristics affected by high temperature/high frequency, though there were no much research upon it behaving with both temperature and frequency.

in Fig3.3 and Fig3.4 we present the different temperature/frequency effects on output impedance z_{out} on both real and imaginary parts

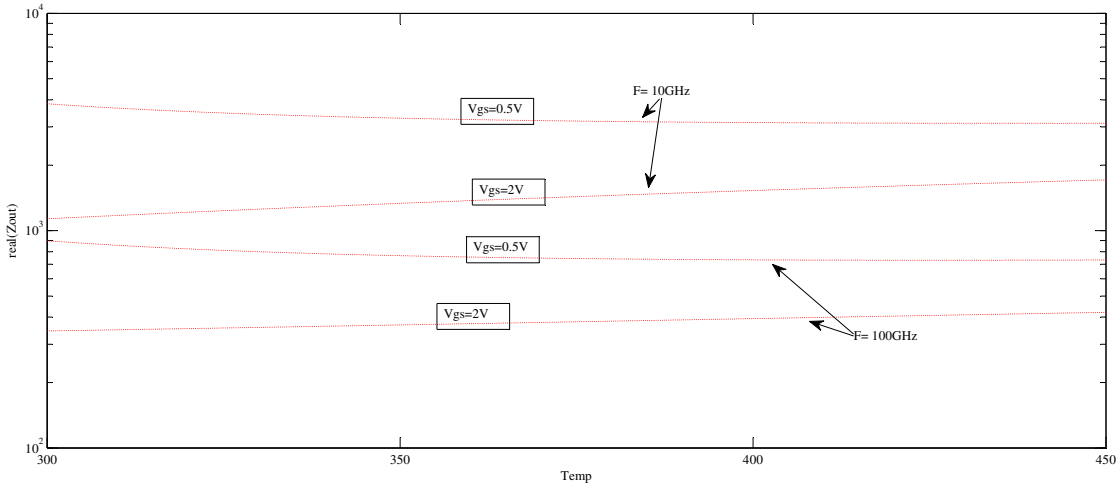


Fig. 3.3: real part of output impedance z_{out} Vs different temperature and frequency

For better recognition of high frequency effect, we show in Fig the output Vs different voltages for real and imaginary parts Getting more with the importance of output impedance and how it is affected by temperature change, In [9] which contain our model, the current relationship (for saturation region) presented was:

$$I_{ds} = WQ(V = V_{dssat})_{v_{sat},ns}$$

this relationship shows the direct effect on I_{ds} current from saturation velocity which was related before with temperature effect, hence now we know how output impedance was affected from its relationship with current. Here in DG mosfet from Fig3.5 and Fig3.6 we can see how imaginary and real part are affected by Temperature with lowering the real part and increasing imaginary part which physically should mean decreasing current and increasing output capacitances, that would be right as we already know that high temperature cause thermal capacitance to appear.

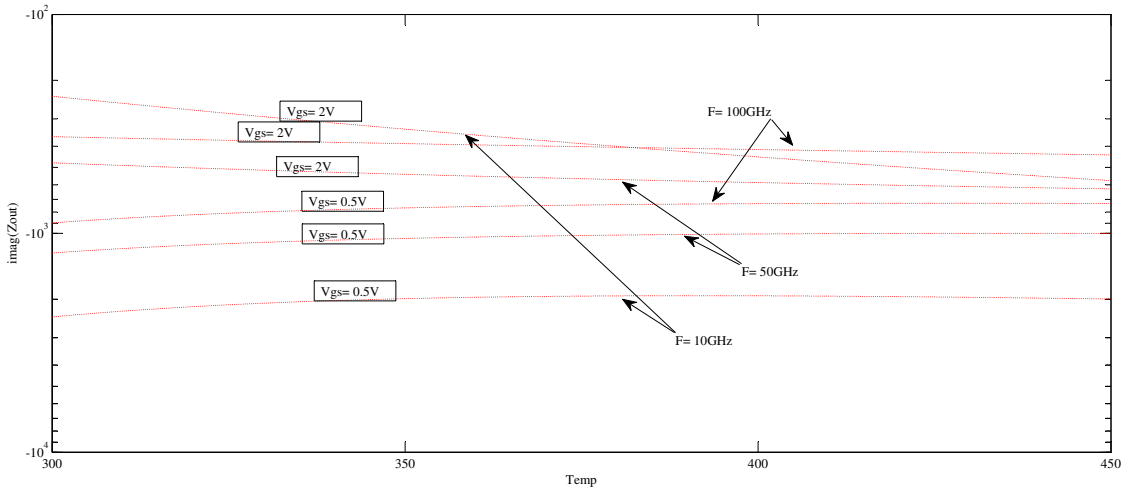


Fig. 3.4: imaginary part of output impedance z_{out} Vs different temperature and frequency

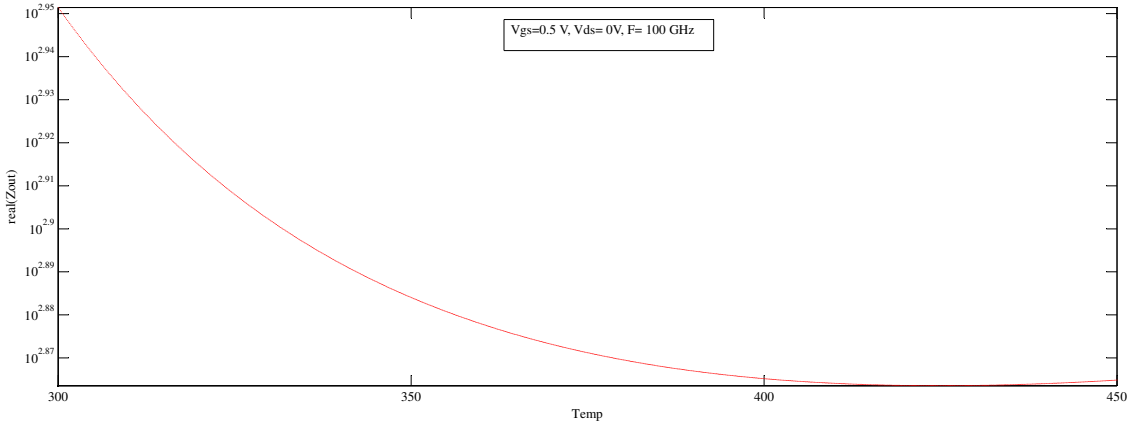


Fig. 3.5: real part of output impedance z_{out} with high frequency $F = 100$GHz and low gate voltage$V_{gs} = 0.5$ V

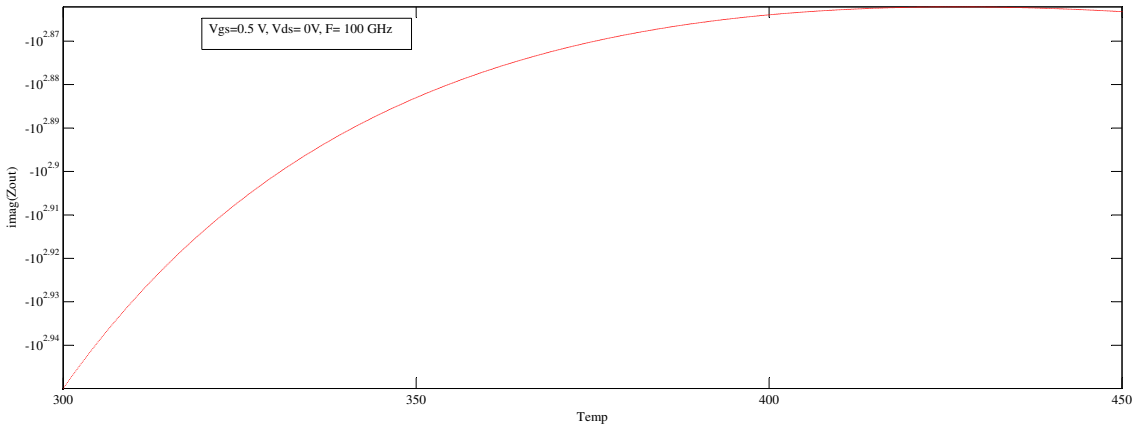


Fig. 3.6: imaginary part of output impedance z_{out} with high frequency F = 100GHz and low gate voltage$V_{gs} = 0.5$ V

Input impedance

To maintain the leakage current very low, output resistance should be high and input resistance should be low [15]. On resistance or the real part of our input resistance had the effect of being increased by temperature but on the other hand lowered by higher frequency shown in Fig3.7, the figure also shows the effect of gate voltage V_{gs} and for the imaginary part shown in Fig3.8 and for more precise results with different range of temperature and only high frequency shown in both Fig3.9 and Fig3.10.

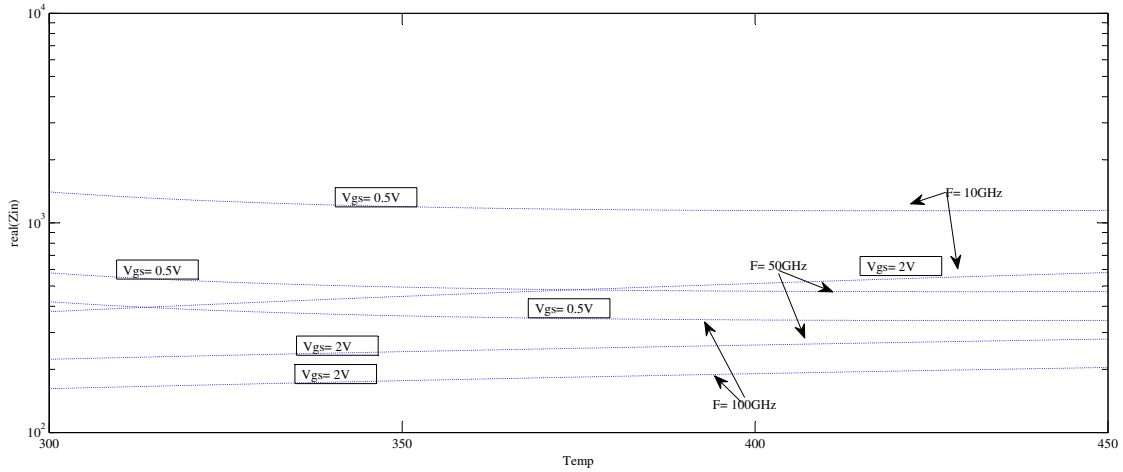


Fig. 3.7: real part of input impedance z_{in} with range of frequencies and range of gate voltage

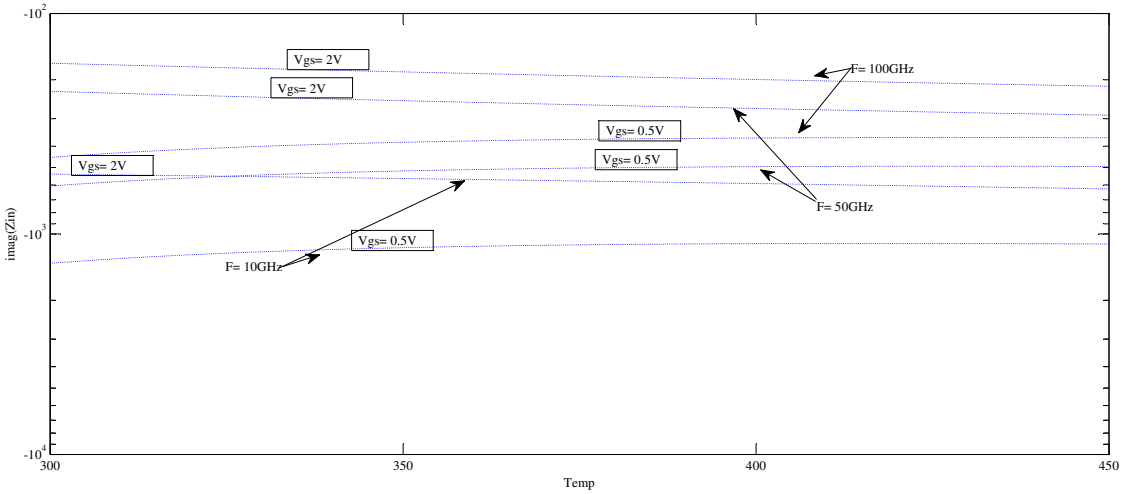


Fig. 3.8: imaginary part of input impedance z_{in} with range of frequencies and range of gate voltage

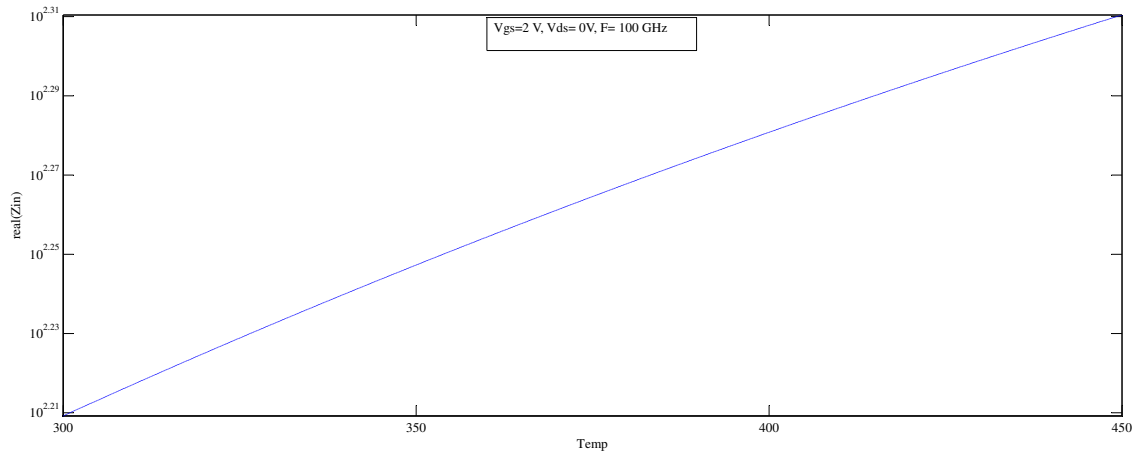


Fig. 3.9: Real part of input impedance only with high frequency high gate voltage

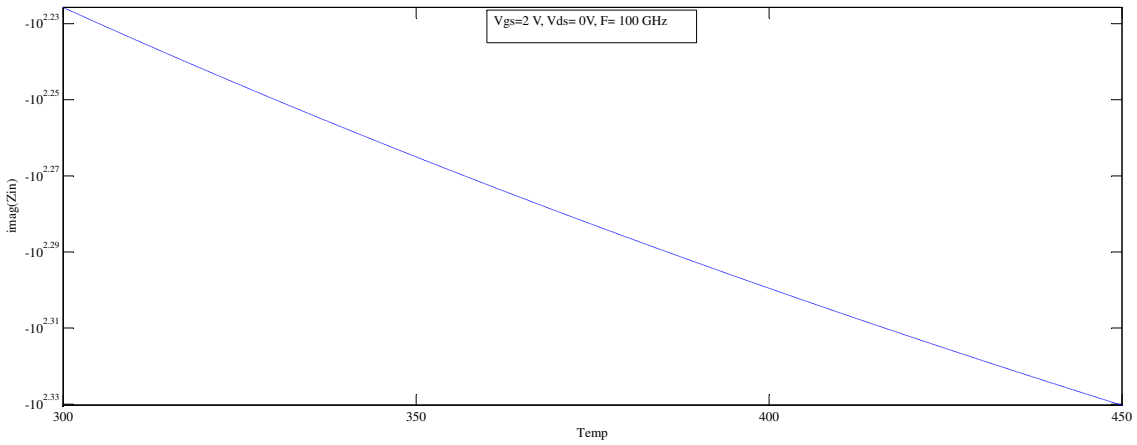


Fig. 3.10: imaginary part of input impedance only with high frequency high gate voltage

Input impedance Vs output resistance

The input impedance over output conductance $z_{in}/R_{out}(10Hz)$ was potted Vs frequencies with different temperature and gate voltage, the resultant Fig3.11 shows that for different temperatures the output deceases gradually for low frequencies with factor $1/F$ and for high frequencies with factor $1/\sqrt{F}$. also in Fig3.14 shows the output conductance changing with temperature with different gate frequencies.

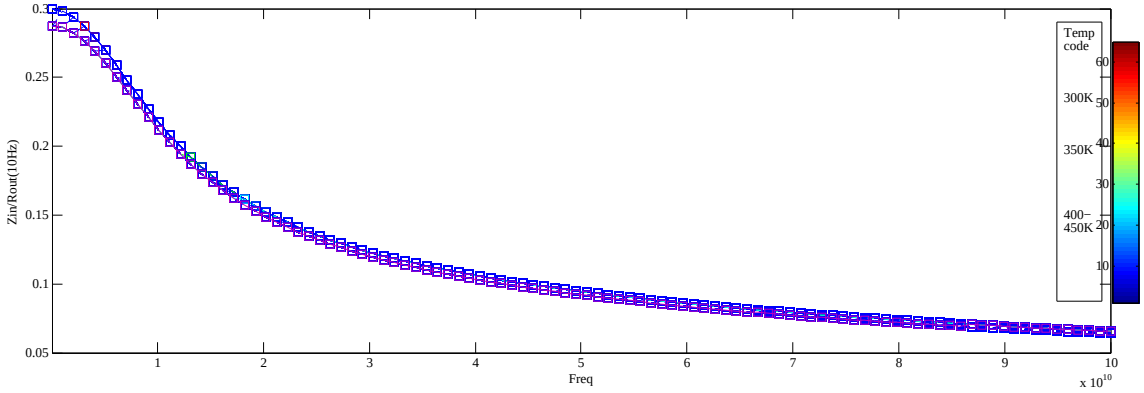


Fig. 3.11: Input impedence/ output conductance Vs frequency

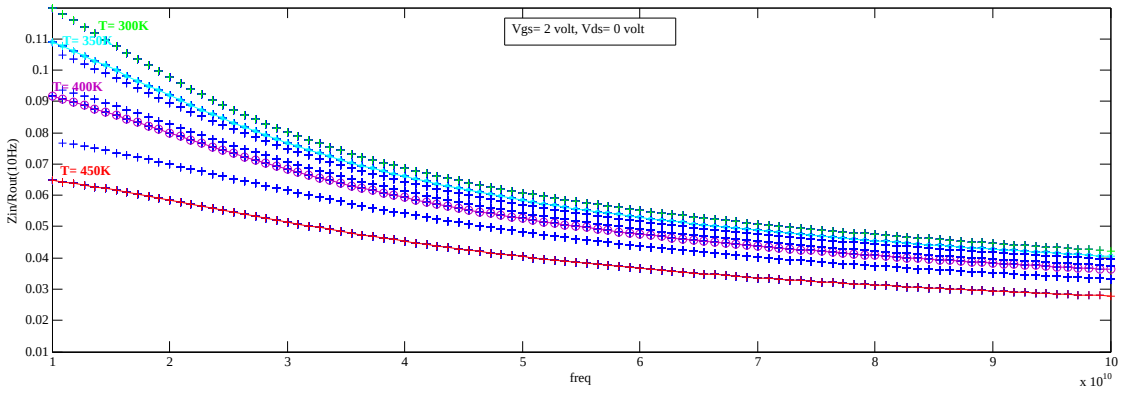


Fig. 3.12: Input impedence/ output conductance Vs frequency for $V_{gs} = 2$ V

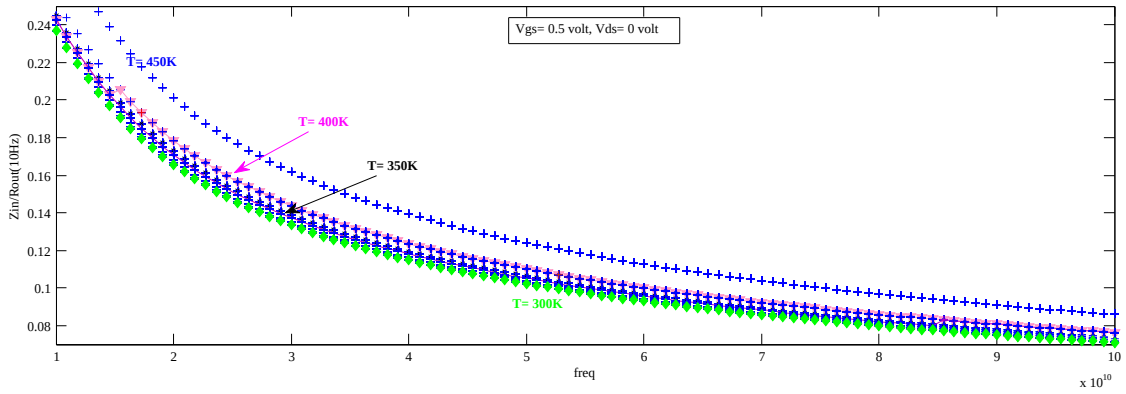


Fig. 3.13: Input impedance/output resistance Vs frequency for $V_{gs} = 0.5$ V

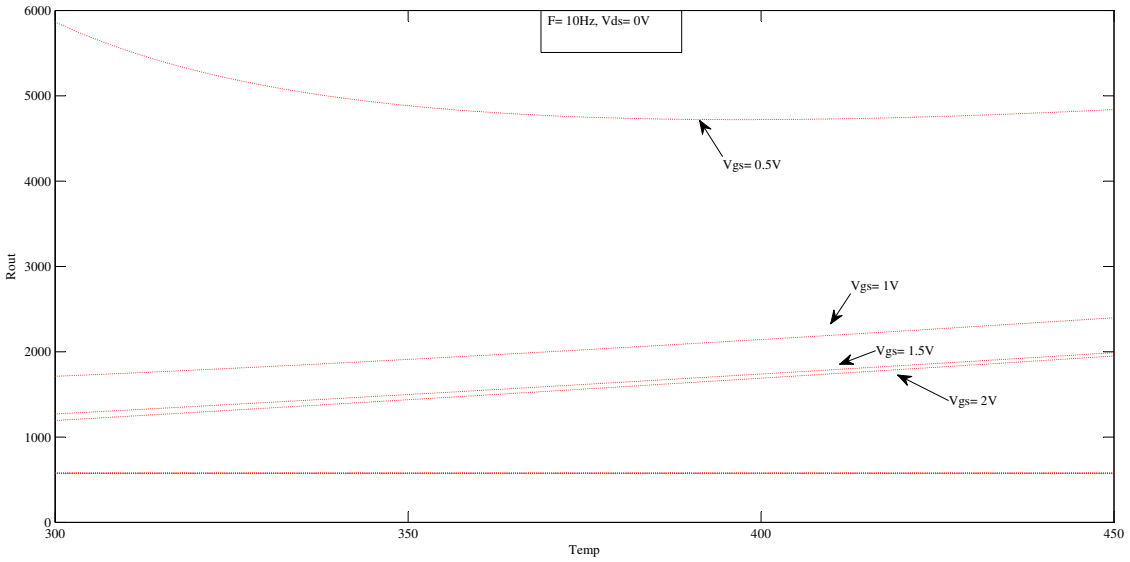


Fig. 3.14: Output conductance with$F = 10Hz$ and range of gate voltage $0.5 < V_{gs} < 2$Volts Vs temperature

3.2 conclusion

As a conclusion we can see from the previous simulation figures, temperature has high effect on DG MOSFETS or on MOSFETS as a total. This effect lowering the behaviour of the DG MOSFETS gradually with high frequency. it was too important to do the analysis in this area, the reason is with the continuous down-scaling and the increase of number of transistors into one single chip, moreover the need of higher performances which means higher frequency. This increasing number of transistor into one single chips eventually leads to the increase of temperature, hence introducing those limiting effects.

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